

## Optimum FIR Filters for Digital Pulse Compression of Biphase Barker Codes with Low Sidelobes

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### Abstract

In Wireless signals and Radar signals where power, real estate, speed and low cost are tight constraints and Doppler tolerance is not a major concern biphase codes are popular and FIR filter is used for digital pulse compression (DPC) implementation to achieve required range resolution. Disadvantage of low peak to sidelobe ratio (PSR) of biphase codes can be overcome by linear programming for either single stage mismatched filter or two stage approach i.e. matched filter followed by sidelobe suppression filter (SSF) filter. Linear programming (LP) calls for longer filter lengths to obtain desirable PSR. Longer the filter length greater will be the number of multipliers, hence more will be the requirement of logic resources used in the FPGAs and many times becomes design challenge for system on chip (SoC) requirement.

This requirement of multipliers can be brought down by clustering the tap weights of the filter by kmeans clustering algorithm at the cost of few dB deterioration in PSR. The cluster centroid as tap weight reduces logic used in FPGA for FIR filters to a great extent by reducing number of weight multipliers. Since kmeans clustering is an iterative algorithm, centroid for weights cluster is different in different iterations and causes different clusters. This causes difference in clustering of weights and sometimes even it may happen that lesser number of multiplier and lesser length of filter provide better PSR.

In this paper few sample optimum biphase codes have been provided in tabular form with their optimum sidelobe suppression filter (SSF) with optimum lengths and minimum multipliers to achieve low sidelobe level of -35 dB to -40 dB and have been compared against PSR achieved without clustering. Clustering is used in FIR filter for pulse compression and its effect is seen on peak to sidelobe ratio. This is being a generic method for FIR filters to reduce number of multipliers can be extended to other similar applications.

**Index Terms**— Digital Pulse Compression (DPC), FIR filter, range sidelobes, sidelobe suppression filter (SSF), range sidelobe reduction, Kmeans algorithm, clustering, centroid, biphase codes, peak to sidelobe ratio (PSR).

### I. INTRODUCTION

Even though biphase codes are used for digital pulse compression in radars and wireless applications for quite some time and various methods have been suggested in literature to reduce their peak to sidelobe ratio, still designer struggles to achieve low peak to sidelobe ratio for biphase codes in the absence of readily available sidelobe suppression filter design methodology and its efficient implementation method. In applications where system is supposed to be built on a single chip in order to meet the specifications of real estate, power, cost and speed, each and every module of the system has to be efficient implementation wise. Efficient implementation of DPC has been suggested in [4] for 13 bit barker code but it is quite exhaustive to group the multipliers when SSF length increases and inefficient grouping of multiplier weights causes severe degradation in PSR, achieved with linear programming. So a method has been evolved to achieve optimal solution, taking care of all the constraints. Kmeans is an algorithm finds application

in image processing for clustering of data, has been used to provide solution to cluster the multipliers used as tap weights for efficient implementation and without much degradation in PSR.

Iterative Kmeans algorithm causes difference in clustering of weights in each iteration and sometimes even it may happen that lesser number of multiplier and lesser length of filter provide better PSR. Optimum length of SSF with minimum multipliers to achieve minimum PSR is desirable. However when all the multipliers will be implemented, there will be no deterioration in PSR achieved with linear programming provided overall design fits in the FPGA. This approach is useful in applications where System on Chip (SoC) via FPGA is supposed to be realized or in applications where design is being finalized for ASIC for bulk production, so logic required for each module of system should be minimum.

### II. RANGE SIDELOBE SUPPRESSION FOR TWO STAGE APPROACH

Range sidelobe suppression in DPC for biphasic codes can be achieved by single stage mismatched filter or by two stage approach as shown in figure 1. Paper provides solution for two stage approach and optimal SSF filter design.

Multiplier weights for single stage filter can also be achieved in similar manner.

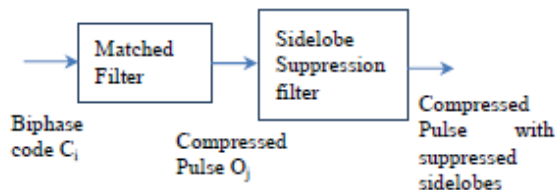


Figure (1) : Two stage approach

Sidelobe suppression filter is designed in two steps. In first step its multiplier weights are obtained by linear programming. In next step multiplier weights are grouped together by kmean clustering algorithm to bring down multipliers requirement. Multiplier weights obtained offline can be stored in memory to be used as shown in figure 2 for column 3 of table 2 with 6 weights.

### III. DESIGN STEPS OF SSF

#### Linear programming

In step one linear programming technique of optimization is used to compute filter tap weights for binary phase coded waveforms.

Transmitted binary code,

$$C_i = \pm 1, 1 \leq i \leq N.$$

Pulse compression filter output,

$$O_j, 1 \leq j \leq 2N-1.$$

Sidelobe suppression filter tap weights,

$$S_j, 1 \leq j \leq M, M \geq 2N-1.$$

$$C_i = 0 \text{ if } i < 1 \text{ or } i > N. \text{ Similarly, } O_j = 0 \text{ if } j < 1$$

$$\text{or } j > 2N-1.$$

To obtain the tap weights for SSF constraints can be given as below.

$$\text{Maximize } \sum_{j=1}^M S_j O_{j-(M-2N+1)/2} \quad (1)$$

$$\text{Subject to } \left| \sum_{i=1}^M S_j O_{j-k} \right| \leq P$$

$$2(1-N) \leq k \leq (M-1), k \neq (M-2N+1)/2$$

Where p is the max sidelobe level for the code at compression filter output. The objective function to be maximized in equation (1) is the mainlobe response of transmitted waveform centered in the filter weights. Equation 1 is having linear objective function with M variables and more than M linear inequality constraints and can be solved by simplex algorithm of linear programming.

#### Kmeans algorithm

In step two k-means clustering [10] has been used to get centroid to be used as tap weight. K-means is a two-phase iterative algorithm to minimize the sum of point-to-centroid distances, summed over all K clusters. Thus, the first phase is thought of as providing a fast but potentially only approximate solution as a starting point for the second phase. In second phase points are individually reassigned if doing so will reduce the sum of distances, and cluster centroids are recomputed after each reassignment.

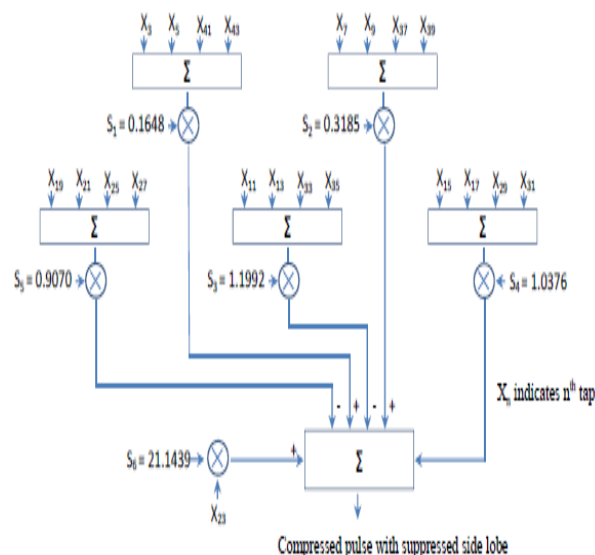


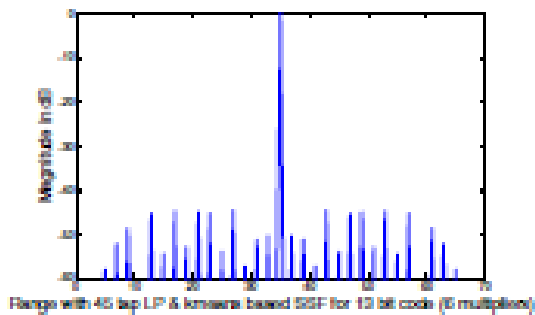
Figure (2) - 46 Tap sample SSF implementation for 13 bit code

To achieve approximately -40 dB PSR via optimum solution in terms of minimum SSF length and minimum multipliers exhaustive search is done for

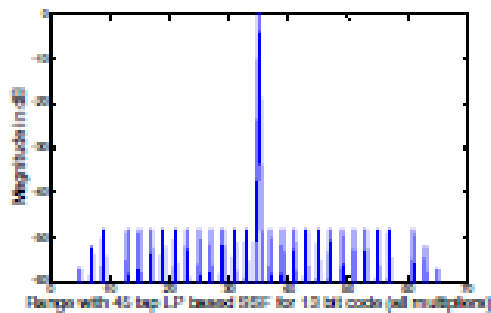
biphase codes mentioned in table 1 and few optimized results are tabulated in tables 2-4. Hardware implementation of sample SSF has been shown in figure 2.

**Table 1 Biphase Code used**

Code Length (Bit)	Biphase Code (hex)
13	1F35
25	1CE0549
51	71C077376ADB4
73[2]	1E78C0224973217C4E4
83[2]	4463BBF70F17E24FA4ADA
99[2]	63912B7FDB06B5268FAA8D71



**Figure 3(b)**



**Figure 3(a)**

It can be noted from table 2, that for odd lengths of SSF, multiplier weights are symmetrical on both sides of middle tap weight while for even length of SSF, multiplier weights may or may not be symmetrical on both sides of middle tap weight. Hence, for 25 and 85 bit codes mentioned in table 1, SSF weights have been provided for odd SSF lengths up to middle tap weight in table 3.

**Table 2 - Multiplier weights for 13 bit biphase code**

Index	LP based 45 tap SSF Multiplier PSE=-48.37 dB	LP & kmeans based 45 tap SSF 6 Multiplier PSE=-44.52 dB	LP & kmeans based 45 tap SSF 9 Multiplier PSE=-45.19 dB	LP & kmeans based 48 tap SSF 8 Multiplier PSE=-44.35 dB	LP & kmeans based 44 Tap SSF 8 Multiplier PSE=-43.40 dB	LP & kmeans based 42 tap SSF 10 Multiplier PSE=-46.83 dB	LP & kmeans based 37 Tap SSF 10 Multiplier PSE=-43.46 dB	LP based 37 Tap Multiplier PSE=-43.13 dB	LP & kmeans based 37 Tap SSF 4 Multiplier PSE=-40.0 dB
1	0.0332	0.0000	0.0028	-0.0049	-0.0000	0.0885	0.1291	0.2222	0.2811
2	-0.0000	0.0000	-0.0028	0.0049	0.1371	0.0000	0.0000	-0.0000	0
3	0.1235	0.1648	0.1235	0.0049	-0.0000	0.1696	0.1291	0.2724	0.2811
4	-0.0000	0.0000	-0.0028	0.1694	0.1371	-0.0000	-0.0000	0.0000	0
5	0.2061	0.1648	0.2430	0.0049	-0.0000	0.2690	0.3709	0.3164	0.2811
6	-0.0000	0.0000	-0.0028	0.1694	0.2509	0.0000	0.0000	0.0000	0
7	0.2798	0.3185	0.2430	-0.0049	-0.0000	0.4729	0.3709	-0.6498	-1.1609
8	-0.0000	0.0000	-0.0028	0.3298	0.4821	-0.0000	-0.0000	0.0000	0
9	0.3573	0.3185	0.3573	0.0049	-0.0000	-1.0470	-1.0089	-0.6057	-1.1609
10	-0.0000	0.0000	-0.0028	0.3298	-1.0345	-0.0000	-0.0000	-0.0000	0
11	-1.2380	-1.1992	-1.1992	0.0049	-0.0000	-0.9708	-1.0089	-0.5556	-1.1609
12	0.0000	0.0000	0.0028	-1.2383	-0.9283	-0.0000	-0.0000	-0.0000	0
13	-1.1605	-1.1992	-1.1992	0.0049	-0.0000	-1.0470	-1.0089	-0.6667	-0.9351
14	-0.0000	0.0000	-0.0028	-1.1674	-1.0345	-0.0000	-0.0000	0.0000	0
15	-1.0841	-1.0376	-1.0841	-0.0049	-0.0000	-0.9708	-1.0089	-0.6019	-0.9351
16	-0.0000	0.0000	-0.0028	-1.0524	-1.0345	0.0000	0.0000	0.0000	0
17	-0.9912	-1.0376	-0.9607	-0.0049	0.0000	-0.8709	-0.8709	-0.5287	-0.9351
18	-0.0000	0.0000	-0.0028	-1.0524	-0.9283	0.0000	0.0000	0.0000	0
19	-0.8837	-0.9070	-0.8837	-0.0049	0.0000	-0.7679	-0.7679	11.5944	21.1439
20	0.0000	0.0000	0.0028	-0.8521	-0.7807	0.0000	0.0000	-0.0000	0
21	-0.9303	-0.9070	-0.9607	-0.0049	0.0000	18.0584	18.0584	-0.5287	-0.9351
22	0.0000	0.0000	0.0028	-0.8521	18.1773	0.0000	0.0000	-0.0000	0
23	21.1439	21.1439	21.1439	-0.0049	0.0000	-0.7679	-0.7679	-0.6019	-0.9351
24	0.0000	0.0000	0.0028	21.2314	-0.7807	0.0000	0.0000	-0.0000	0
25	-0.9303	-0.9070	-0.9607	0.0049	-0.0000	-0.8709	-0.8709	-0.6667	-0.9351
26	0.0000	0.0000	0.0028	-0.8521	-0.7807	-0.0000	-0.0000	0.0000	0
27	-0.8837	-0.9070	-0.8837	0.0049	-0.0000	-0.9708	-1.0089	-0.5556	-1.1609
28	-0.0000	0.0000	-0.0028	-1.0524	-0.7807	0.0000	0.0000	0.0000	0
29	-0.9912	-1.0376	-0.9607	0.0049	0.0000	-1.0470	-1.0089	-0.6057	-1.1609
30	0.0000	0.0000	0.0028	-1.1674	-0.9283	-0.0000	-0.0000	-0.0000	0
31	-1.0841	-1.0376	-1.0841	0.0049	-0.0000	-0.9708	-1.0089	-0.6498	-1.1609
32	-0.0000	0.0000	-0.0028	-1.0524	-1.0345	-0.0000	-0.0000	-0.0000	0
33	-1.1605	-1.1992	-1.1992	0.0049	-0.0000	-1.0470	-1.0089	0.3164	0.2811
34	-0.0000	0.0000	-0.0028	-1.1674	-1.0345	-0.0000	-0.0000	0.0000	0
35	-1.2380	-1.1992	-1.1992	0.0049	-0.0000	0.4729	0.3709	0.2724	0.2811
36	-0.0000	0.0000	-0.0028	-1.2383	0.2509	-0.0000	-0.0000	0.0000	0
37	0.3573	0.3185	0.3573	0.0049	0.0000	0.2690	0.3709	0.2222	0.2811
38	-0.0000	0.0000	-0.0028	0.3298	0.2509	0.0000	0.0000	0.0000	0
39	0.2798	0.3185	0.2430	0.0049	0.0000	0.1696	0.1291	0.0000	0
40	-0.0000	0.0000	-0.0028	0.3298	0.1371	0.0000	0.0000	0.0000	0
41	0.2061	0.1648	0.2430	0.0049	-0.0000	0.0885	0.1291	0.0000	0
42	-0.0000	0.0000	-0.0028	0.1694	0.1371	0.0000	0.0000	0.0000	0
43	0.1235	0.1648	0.1235	-0.0049	-0.0000	0.0000	0.0000	0.0000	0
44	-0.0000	0.0000	-0.0028	0.1694	0.1371	0.0000	0.0000	0.0000	0
45	0.0332	0.0000	0.0028	-0.0049	-0.0049	0.0000	0.0000	0.0000	0
46				0.0049	0.0049	0.0000	0.0000	0.0000	0
47				-0.0049	-0.0049	0.0000	0.0000	0.0000	0
48				-0.0049	-0.0049	0.0000	0.0000	0.0000	0

**IV. SIMULATION RESULTS**

Figure 4(a) and 4(b) shows range vs magnitude plot for 25 bit biphase code for 85 tap SSF for LP and LP & kmeans based SSF respectively, figure 5(a) and 5(b) shows range vs magnitude plot for 83 bit biphase code for 219 tap SSF for LP and LP & kmeans based SSF respectively. Figure 4(c) shows compressed pulse widths at the output of LP vs LP & kmeans based 85 tap SSF for 25 bit code, it can be seen that compressed pulse width doesn't change with LP and kmeans based SSF. Figure 5(c) shows compressed pulse at the output of LP vs LP & kmeans based 219 tap SSF for 83 bit code, same can be noted from figure 5(c) too that compressed pulse width remains unchanged with LP & kmeans based SSF.

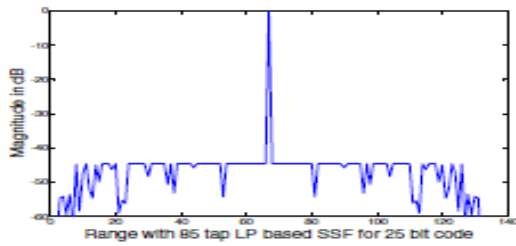


Figure 4(a)

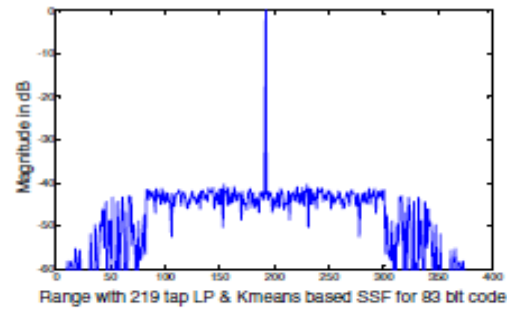


Figure 5(b)

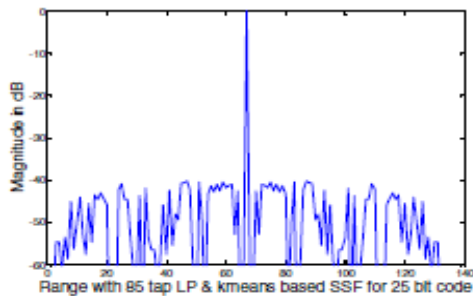


Figure 4(b)

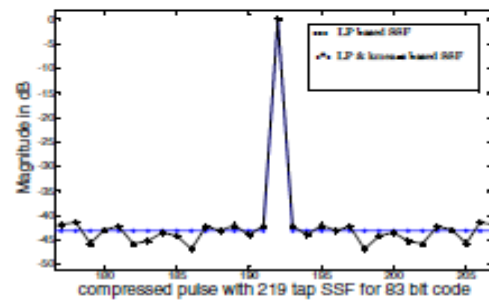


Figure 5(c)

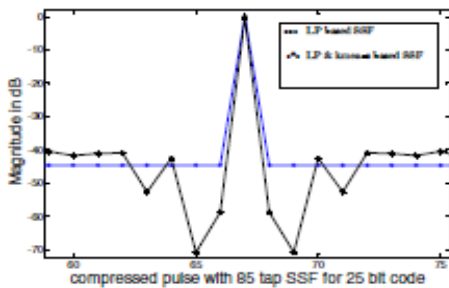


Figure 4(c)

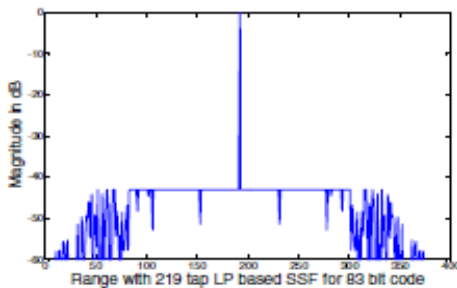


Figure 5(a)

Table 3 – SSF tap weights for 25 & 83 bit code

Index	LP based 85 tap SSF 43 Multipliers PSR= -44.66 dB		LP & kmeans based 85 tap SSF 9 Multiplier PSR= -40.17dB		LP based 219 tap SSF 110 Multipliers PSR= -43.08 dB		LP & kmeans based 219 tap SSF 18 Multiplier PSR= -40.37dB	
	Multiplier Weight for 25 bit code	Multiplier Weight for 25 bit code	Multiplier Weight for 83 bit code	Multiplier Weight for 83 bit code	Multiplier Weight for 83 bit code	Multiplier Weight for 83 bit code	Multiplier Weight Index	
1	0.2960	0.3213	0.0645	0.0520	11			
2	0.1255	0.1169	-0.0307	-0.0134	3			
3	-0.3293	-0.3213	-0.0865	-0.0913	4			
4	0.0507	0.1169	-0.0004	-0.0134	3			
5	0.5816	0.5218	-0.0464	-0.0520	11			
6	-0.3629	-0.3213	0.0533	0.0520	11			
7	0.0950	0.1169	-0.0972	-0.0913	4			
8	0.2584	0.3213	0.1798	0.1818	5			
9	-0.1135	-0.1169	-0.0207	-0.0134	3			
10	0.2623	0.3213	0.1199	0.1323	14			
11	0.1917	0.1169	-0.0572	-0.0520	11			
12	-0.2020	-0.1169	0.0886	0.0913	4			
13	0.4804	0.5218	-0.0153	-0.0134	3			
14	0.1455	0.1169	0.0235	0.0134	3			
15	-0.1053	-0.1169	-0.0738	-0.0913	4			
16	0.1901	0.1169	0.0950	0.0913	4			
17	0.1444	0.1169	-0.0403	-0.0520	11			
18	0.0093	0.1169	0.0672	0.0520	11			

19	-0.0890	-0.1169	-0.0494	-0.0520	11
20	0.0395	0.1169	0.0966	0.0913	4
21	-0.1115	-0.1169	-0.0586	-0.0520	11
22	1.9624	1.9267	-0.0034	-0.0134	3
23	0.3754	0.3213	0.1173	0.1323	14
24	-1.4612	-1.4163	-0.0109	-0.0134	3
25	1.1472	1.2054	0.0470	0.0520	11
26	1.3275	1.4163	0.0573	0.0520	11
27	-0.8788	-0.8134	0.1506	0.1323	14
28	1.4602	1.4163	0.0487	0.0520	11
29	-0.3218	-0.3213	-0.2787	-0.2705	15
30	0.7988	0.8134	0.3156	0.3072	7
31	1.2636	1.2054	-0.2352	-0.2156	16
32	-0.1173	-0.1169	0.1382	0.1323	14
33	0.1395	0.1169	0.0397	0.0520	11
34	0.8471	0.8134	0.3109	0.3072	7
35	0.3644	0.3213	-0.4128	-0.3988	18
36	-1.0473	-1.0005	0.3945	0.3988	18
37	0.9865	1.0005	0.1236	0.1323	14
38	-0.9678	-1.0005	0.0786	0.0913	4
39	0.4433	0.5218	-0.4281	-0.4523	2
40	1.8910	1.9267	0.3619	0.3557	13
41	-0.7289	-0.8134	0.2020	0.2156	16
42	-0.3819	-0.5218	0.2996	0.3072	7
43	15.9606	15.9606	-0.3696	-0.3557	13
44			-0.0583	-0.0520	11
45			0.0894	0.0913	4
46			-0.2029	-0.2156	16
47			0.0364	0.0520	11
48			-0.3533	-0.3557	13
49			0.2219	0.2156	16
50			-0.3386	-0.3557	13
51			-0.2074	-0.2156	16
52			0.4048	0.3988	18
53			0.0436	0.0520	11
54			-0.1277	-0.1323	14
55			0.1363	0.1323	14
56			0.0494	0.0520	11
57			-0.3893	-0.3988	18
58			-0.0694	-0.0520	11
59			0.1921	0.1818	5
60			-0.3966	-0.3988	18
61			-0.2695	-0.2705	15
62			0.2352	0.2156	16
63			-0.4760	-0.4523	2
64			0.0796	0.0913	4
65			-0.1921	-0.1818	5
66			0.3026	0.3072	7
67			-0.1064	-0.0913	4
68			0.3889	0.3988	18
69			0.3412	0.3557	13
70			-0.2097	-0.2156	16
71			-0.1342	-0.1323	14
72			-1.0385	-1.0135	9
73			-0.0042	-0.0134	3
74			0.3635	0.3557	13
75			0.2842	0.2705	15
76			-0.1528	-0.1323	14
77			0.0827	0.0913	4

78			0.3852	0.3988	18
79			-1.0214	-1.0135	9
80			-0.5985	-0.6077	8
81			0.4217	0.3988	18
82			0.5931	0.6077	8
83			-0.5299	-0.5392	1
84			0.2627	0.2705	15
85			-0.3950	-0.3988	18
86			-0.0554	-0.0520	11
87			-0.8298	-0.8298	10
88			0.9804	1.0135	9
89			0.1869	0.1818	5
90			0.1016	0.0913	4
91			-0.1407	-0.1323	14
92			-0.0609	-0.0520	11
93			-0.1143	-0.1323	14
94			0.0112	0.0134	3
95			-0.1636	-0.1818	5
96			-0.0377	-0.0520	11
97			0.1092	0.0913	4
98			0.4520	0.4523	2
99			-0.1761	-0.1818	5
100			-0.0793	-0.0913	4
101			0.1102	0.0913	4
102			-0.0867	-0.0913	4
103			0.7487	0.7487	17
104			0.6314	0.6077	8
105			-0.3616	-0.3557	13
106			0.4532	0.4523	2
107			-0.2574	-0.2705	15
108			-0.2105	-0.2156	16
109			-0.5485	-0.5392	1
110			11.8514	11.8514	6

Table 4 – 13, 25, 51, 73, 83, 99 bit code results

Code length (bit)	SSP length tap	With LP PSIR (dB)	Min fil- piers required	With LP & Kramers PSIR (dB)	Min fil- piers required
13	37	-43.13	10	-43.06	10
	38	-43.13	10	-42.93	9
	41	-46.98	11	-44.87	9
	41	-46.98	11	-42.15	6
	41	-46.98	11	-40.91	5
	45	-48.37	12	-44.32	7
	45	-48.37	12	-42.82	6
	49	-48.63	13	-45.16	8
25	85	-44.66	43	-40.17	9
	87	-46.38	44	-42.26	12
	89	-46.51	45	-44.24	23
	90	-46.51	90	-43.17	19
	91	-46.51	46	-41.66	16
	93	-46.88	47	-45.00	22
	97	-47.03	49	-40.32	11
	97	-47.03	49	-45.19	25

31	175	-41.95	88	-41.01	39
	177	-42.68	89	-40.00	28
	179	-42.76	90	-41.27	38
	183	-42.93	92	-40.58	26
	183	-42.93	92	-41.38	36
	199	-43.44	100	-40.13	23
	199	-43.44	100	-41.88	39
	199	-43.44	100	-42.49	46
	201	-43.48	101	-41.15	29
73	223	-41.33	113	-40.33	52
	237	-42.21	119	-40.10	30
	264	-43.32	264	-40.63	41
	269	-43.46	133	-40.02	39
	272	-43.71	272	-40.21	36
	273	-43.91	137	-40.10	23
	273	-43.91	137	-40.83	31
	273	-43.91	137	-41.36	45
	273	-43.91	137	-42.43	37
	274	-43.91	274	-40.27	25
	274	-43.91	274	-41.64	54
	275	-43.92	138	-40.00	22
	275	-43.92	138	-41.14	37
	275	-43.92	138	-42.04	33
	281	-44.31	141	-40.23	37
	281	-44.31	141	-41.43	32
	281	-44.31	141	-42.00	60
	281	-44.31	141	-43.03	64
	289	-44.37	145	-40.27	40
83	177	-40.01	89	-39.30	38
	205	-41.36	103	-40.02	31
	207	-42.26	104	-40.30	25
	219	-43.08	110	-40.37	18
	233	-44.43	128	-40.40	15
	287	-45.82	144	-40.76	13
	211	-42.39	106	-41.03	33
	216	-42.77	216	-41.48	34
	223	-43.16	113	-41.18	25
	234	-44.42	234	-41.23	19
	288	-45.82	288	-41.12	16
	228	-43.19	228	-42.17	37
	231	-44.34	126	-42.48	27
	293	-46.39	148	-42.93	23
	323	-47.18	163	-42.90	20
	326	-47.19	326	-42.10	15
	251	-44.34	126	-43.08	38
	279	-45.10	140	-43.00	33
	293	-46.39	148	-43.04	32
	330	-47.23	330	-43.71	24
	287	-45.82	144	-44.39	46
	306	-46.62	306	-44.00	38
	330	-47.23	330	-44.39	30
	293	-46.39	148	-45.30	63
	311	-46.65	156	-45.00	37
	321	-47.09	161	-45.01	45
99	368	-40.11	368	-36.41	79
	367	-40.38	184	-38.31	76

	381	-41.18	191	-39.07	70
	381	-41.18	191	-39.64	84
	381	-41.18	191	-39.14	65
	419	-41.96	210	-40.02	104
	423	-42.00	212	-39.11	79
	429	-42.07	213	-40.22	103
	437	-42.16	219	-40.04	88
	437	-42.16	219	-40.69	108
	439	-42.24	220	-40.51	95
	473	-42.87	238	-40.06	95
	473	-42.87	238	-40.47	106
	491	-43.18	246	-40.68	118

### V. CONCLUSION

Biphase and polyphase codes will never be out of fashion in DPC, irrespective of radar history as they are foundation stone of DPC. In applications where Doppler tolerance is not a major concern biphase codes are preferred over polyphase codes for their simplicity. Fast Convolution is preferred over FIR filters for digital pulse compression in radars for computational advantage for longer codes and range gates in digital signal processing. However for FPGA based implementation of matched filter along with SSF for longer biphase codes, poses constraint over logic resources used. The proposed optimization solution paves a way to reduce hardware in the current generation of radar where multiple simultaneous beams are formed. Multiple simultaneous beams in radars play important role, especially in difficult to detect and multi target environment. This method of reducing number of multiplier is applicable to polyphase codes too. But polyphase codes do not have choice to improve PSR using longer length SSF; code length and incorporation of window at receiver determines PSR. Achieved PSR deteriorates a bit because of clustering.

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